REMARKS

Claims 1-26 were pending and under consideration.

In the Office Action of March 11, 2008, claims 1-26 were rejected. An objections was raised against the drawings.

In response, claims 1-5, 12 and 19 have been cancelled, claims 6-11, 13-18 and 20-26 have been amended, and Figures 11 and 12 have been amended as requested.

Regarding the rejections of the claims 6-9 and 20-23 as anticipated by Mori et al, (US 7102680), independent claims 6 and 20 have been amended to recite, respectively, a CMOS imager structure and a driving method used for the structure, in which the structure includes a plurality of pixels, each pixel comprising:

(a) a photoelectric conversion element formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light;

(b) a readout section formed in said well region for reading out the signal charge produced by said photoelectric conversion element at a predetermined readout timing;

(c) a node connecting the photo electric conversion element through the readout section; and

(d) voltage control unit for applying a predetermined substrate bias voltage to said well region upon reading out of the signal charge by said readout section.

With this structure, the claims are directed to CMOS image sensors (CIS). This is because of the readout sections for each pixel.

In contrast, whatever Mori et al may teach, Mori et al is directed to a CCD structure in which the charges from a plurality of pixels are transferred out via a common transfer section. See, e.g., USP 7102680, Col. 3, lines 50-67. As such, Mori et al does not anticipate any of these claims because it fails to provide the necessary pixel readout sections.

Regarding the rejection of claims 13-16 and 25-26 as anticipated by Morimoto. (USP 5729287), whatever else Morimoto may teach, Morimoto is also directed to a CCD image sensor, not the required CMOS image sensor. See, e.g., USP 5729287, Col. 1, lines 6-11. Accordingly, Morimoto cannot anticipate the present claims because it too fails to include the requisite pixel specific readout sections.

Regarding the rejections of claims 10 and 24 as obvious in view of Mori et al and Rhodes (USP 6825878), because Rhodes is directed to CMOS images and not CCDs, there is no suggestion to combine the teachings as the examiner proposes. These are different technologies with different concerns and problems. As such the rejection is improper.

Regarding the rejection of claim 11 as obvious in view of Mori et al and Yanai (USPub 2003/0030737) , whatever else Yanai may teach, it too is directed to CCD imagers and thus cannot cure the deficiencies of Mori et al. Together they fail to anticipate the claimed CMOS imager device technology with pixel-individual readout sections.

Regarding the rejection of claim 18 as obvious in view of Morimoto and Rhodes, this rejection is traversed because, again, the rejection relies on an improper combination of teachings from two different technologies, namely the CCD technology of Morimoto et al and the CMOS imager technology of Rhodes. Because the combination is not suggested due to the different problems and concerns of these technologies, there is no suggestion for the combination.

Regarding the rejection of claim 18 as obvious in view of Morimoto and Yanai, again, both of these are directed to CCD imager technology and not CMOS imager technology and thus fail to suggest the pixel-individual structures as claimed.

In view of the foregoing, it is submitted that claims 6-11, 13-18 and 20-26 are allowable over the cited art and that the application is condition for allowance. Notice to that effect is requested.

Respectfully submitted by,

/David R. Metzger/ (Reg. 32,919)
David R. Metzger
SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, IL 60606-1080
Telephone: 312/876-8000
Fax: 312/876-7934